REMARKS

Introduction

A one-month extension of time to respond to the August 25, 2004 Office Action is hereby respectfully requested. A check in the amount of $120.00 is enclosed in payment of the one-month extension-of-time fee.

The specification has been amended to update an outdated cross-reference to another patent application and to correct a minor and obvious typographical error. Claims 1, 2, 4, and 5 have been amended to more particularly define the invention. Claims 7-39 have been added. Claims 3 and 6 are also in this case. In amended FIG. 6, the type of transistor element 610 has been corrected. No new matter has been added by the amendments to the specification, claims, and drawings.

The drawings have been objected to because of a minor typographical error.

Claims 1-6 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-6 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Nolan et al. U.S. Patent 6,020,792 (hereinafter "Nolan").

Reconsideration and allowance of this application in light of the following remarks is hereby respectfully requested.

The Objections to the Drawings

The Examiner objected to the drawings because of a minor typographical error. In the aforementioned Office Action, the Examiner stated that "transistor (610) in figure 6 is supposed to be an PNP transistor (see spec. page 14)," (Office Action, page 2, lines 1 and 2).

Filed concurrently herewith, please find proposed replacement drawing sheet 6, which corrects this minor typographical error in FIG. 6. This drawing sheet is being filed in response to the Examiner's request in the Office Action mailed on August 25, 2004. No new matter has been added by any of the changes to the drawing sheet.

Applicant's Reply
to the Rejection under 35 U.S.C. § 112

Applicant has amended independent claims 1, 4, and 5 to more particularly point out and describe the claimed invention. No new subject matter has been added by these amendments.

In the aforementioned Office Action, the Examiner stated that the recitations "a first switching threshold is obtainable" and "a second switching threshold is obtainable" in claims 1 and 2 are "confusing because it is [not] clear how the 'first switching threshold' and the 'second switching threshold' can be obtained," (Office Action, page 2, line 23 through page 3, line 1). The Examiner further stated that claims 1 and 2 are indefinite because it is not clear how "the SET and the RESET circuits are maintained," (Office Action, page 3, line 2).

Applicant has amended each of claims 1, 4, and 5 to further point out and define the claimed invention and has amended claim 2 to depend from claim 1.

Applicant has amended each of claims 1, 4, and 5 to state that the latch circuit has a "total current." This total current, which refers to the current internally provided to the overall latch circuit and not to the individual currents flowing through specific portions of said circuit, is recited in the specification at page 7, line 1. In one embodiment shown in the specification, a number of current sources may be utilized to produce this current. See page 3, line 31 through page 4, line 1.

Applicant has also amended claim 1 to state that a "trigger" signal is applied to a particular circuit to change the circuit's output. The trigger signal may cause a voltage change at the application point of the signal which is more than an order of magnitude smaller than the voltage change caused by the conventional current. This trigger signal, the application of which is to change the output of the latch, as described in the specification at page 4, lines 8-17 and at page 4, lines 22-28, causes a substantially smaller voltage rise (e.g., in one embodiment shown in the specification, about 18 millivolts) than does the conventional control signal (e.g., 700 millivolts). See page 8, lines 24-28. Therefore, the rejection of independent claim 1 under 35 U.S.C. § 112 is respectfully traversed. It follows that the rejection of claims 2 and 3 under 35 U.S.C. § 112, which depend from independent claim 1, are also respectfully traversed.

In the aforementioned Office Action, the Examiner stated that the recitations "a first latch transistor", "a second latch transistor", "a SET transistor", and "a RESET transistor" of claim 4 are "indefinite because they can not be identified in the drawing," (Office Action, page 3, lines 10 and 11).

Applicant's invention, as defined by amended independent claim 4 is for a latch circuit having a total current and at least one output, "the output having a first state and a second state," wherein the output is controllable by a "first trigger signal and a second trigger signal," as opposed to conventional control signals. The latch circuit of applicant's claim 4 is shown, for example, in FIG. 2 and includes a SET circuit having a first latch transistor (e.g., transistor 120) and a SET transistor (e.g., transistor 110), a RESET circuit having a second latch transistor (e.g., transistor 130) and a RESET transistor (e.g., transistor 140). Claim 4 defines

this latch circuit, wherein one of the following conditions is true: 1) at the first state, "the total current is conducted by the first latch transistor and the SET transistor wherein the SET transistor switches when the first trigger signal is applied to the SET transistor" and 2) at the second state, "the total current is conducted by the second latch transistor and the RESET transistor wherein the RESET transistor switches when the second trigger signal is applied to the RESET transistor."

At an output state of the claimed latch circuit, one of the SET and RESET transistors of the latch circuit switches when a trigger signal is applied thereto. The latch circuit of the present invention which uses trigger signals has a number of advantages over conventional oscillators such as "high speed operation without the complexity, high device count, and level shifting circuitry associated with ECL," (applicant's specification, page 13, lines 18-20). Therefore, the rejection of independent claim 4 under 35 U.S.C. § 112 is respectfully traversed.

Applicant has also amended method claim 5 to include the application of a "trigger" signal to change the output of the latch circuit by switching one of the SET or RESET transistors. Therefore, the rejection of independent claim 5 under 35 U.S.C. § 112 is respectfully traversed. It follows that the rejection of claim 6 under 35 U.S.C. § 112, which depends from independent claim 5, is also respectfully traversed.

Applicant's Reply
to the Rejections under 35 U.S.C. § 102

Applicant's invention, as defined by amended claim 4, is for a latch circuit having a total current, wherein the output of the of the latch circuit has a first state and a second state, and is changed by the use of a "trigger signal" as opposed to a conventional control

signal. The latch circuit of applicant's claim 4 is shown, for example, in FIG. 2 and includes a SET circuit having a first latch transistor (e.g., transistor 120) and a SET transistor (e.g., transistor 110), a RESET circuit having a second latch transistor (e.g., transistor 130) and a RESET transistor (e.g., transistor 140), wherein one of the following conditions is true: "1) at the first state, the total current is conducted by the first latch transistor and the SET transistor, wherein the SET transistor switches when the first trigger signal is applied to the SET transistor, and wherein the first trigger signal is less than the full Vbe voltage of the SET transistor," and "2) at the second state, the total current is conducted by the second latch transistor and the RESET transistor, wherein the RESET transistor switches when the second trigger signal is applied to the RESET transistor, and wherein the second trigger signal is less than the full Vbe voltage of the RESET transistor."

Each of the SET and RESET transistors of this claimed latch circuit switches when a trigger signal substantially less than the full Vbe voltage of that transistor is applied to that transistor. The latch circuit of the present invention which uses these trigger signals has a number of advantages over conventional latch circuits, such as "high speed operation without the complexity, high device count, and level shifting circuitry associated with ECL [(emitter-coupled logic)]," (applicant's specification, page 13, lines 18-20). Also, see page 9, line 26 through page 10, line 8.

Therefore, applicant respectfully disagrees with the Examiner, who stated that switching thresholds obtainable by trigger signals, as defined by applicant's claim 4, is the "basic function" of a "SET/RESET flip-flop circuit," (Office Action, page 4, line 13. The claimed trigger signals of the present invention can be more than

an order of magnitude smaller than the conventional signal required to change the output of known latch circuits because the required voltage change across the input capacitance is substantially reduced, the threshold value is well-defined by resistor and transistor matching, and, unlike ECL latches, the circuit can operate from a supply as low as one V_{be}. See, for example, applicant's specification, page 5, line 25 through page 6, line 33.

Nolan, on the other hand, simply discloses an oscillator that "produces a stable clock frequency over wide variations of ambient temperature." See Nolan, column 2, lines 29 and 30. The oscillator circuit shown in FIG. 3 of Nolan does not illustrate SET and RESET transistors, as claimed in applicant's amended claim 4, that respectively switch when a trigger signal substantially less than the full Vbe voltage of that transistor is applied to that transistor. Rather, Nolan discusses, with respect to FIG. 3, an oscillator that includes a commonly known set-reset flip-flop 160 coupled to a comparator circuit 180, wherein the comparator circuit is coupled to a reference voltage generator 150 and absolute temperature current generators CTAT 200 and PTAT 300. These current generators 200 and 300 "compensate for the effects that temperature variation has on the internal components of the device" and produce a charging current I_{ccc} 190 "that is nearly independent of temperature," (Nolan, column 2, lines 46-60).

Nowhere does Nolan show or suggest a latch circuit with a SET transistor and a RESET transistor, wherein at least one of the conditions from the group consisting of the following is true: "1) at the first state, . . . the SET transistor switches when the first trigger signal is applied to the SET transistor, and wherein the first trigger signal is substantially less than the full Vbe voltage of the SET transistor, and 2) at the

second state, . . . the RESET transistor switches when the second trigger signal is applied to the RESET transistor, and wherein the second trigger signal is substantially less than the full Vbe voltage of the RESET transistor," as recited in applicant's amended claim 4, such that the output state of the latch may be changed by the application of a "trigger signal" as opposed to a conventional control signal. Instead, Nolan only discloses common set-reset flip-flop 160, which is understood by one skilled in the art to be an ECL latch (i.e., transistors with coupled emitters) and is not known to include a SET and/or RESET transistor that switches by the application of a trigger signal substantially less than the full Vbe voltage of that transistor.

Thus, for at least these reasons, independent claim 4, and any claims dependent therefrom, including new claims 25-37, are allowable over Nolan. Applicant respectfully requests, therefore, that the rejection of claim 4 under 35 U.S.C. § 102(b) be withdrawn.

Furthermore, independent claims 1 and 5, and any claims dependent therefrom, including claims 2, 3, 6, and new claims 7-24, 38, and 39, are allowable over Nolan for at least the same reasons as claim 4 is allowable over Nolan. Applicant respectfully requests, therefore, that the rejection of claims 1-3, 5, and 6 under 35 U.S.C. § 102(b) also be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-39 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 6. This sheet, which includes FIG. 6, replaces the original sheet including FIG. 6. In FIG. 6, the type of transistor element 610 has been corrected.

Attachment: Replacement Sheet; and
Annotated Sheet Showing Changes.

FIG. 6